Vishnu Vardhan K

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Profile Summary

- Trained in VLSI Frontend design and verification through an intensive 6-month program, guided by an industry expert from Microsoft.
- Gained practical exposure to Verilog, SystemVerilog and UVM with a strong emphasis on verification methodologies and best practices.
- Skilled in writing reusable testbenches and implementing constrained random verification to ensure thorough functional coverage.
- Strong understanding of RTL simulation, debugging, and the overall digital design and verification flow.

Education

Sri Shakthi Institute of Engineering and Technology **Oct. 2022 – May 2026**
Bachelor of Engg in Electronics and Communication - CGPA: 8.1 *Coimbatore, Tamil Nadu*

Relevant Coursework

- ASIC Verification
- RTL Design
- Analog Circuit Analysis
- Soc Verification
- RTL Simulation
- Basic Scripting
- Waveform Analysis
- Computer Architecture

Experience

Xchip Technologies **Jun 2025 – Aug 2025**
Design and Verification Intern

- Design and verify RISC-V based SoC components, including a 3-channel DMA architecture and AHB Lite protocol integration.
- Implement and manage round-robin arbitration for efficient I/O request handling, ensuring optimal memory access.
- Develop and test a 5-stage pipelined RISC-V Processor, focusing on load/store architecture and ISA development.
- Conduct simulation and verification using QuestaSim, Xilinx Vivado, and EDA Playground to validate design functionality and timing.

Projects

AHB Lite Protocol Design and Verification | *SystemVerilog, UVM, TCL* **GitHub** **June 2025**

- Developed an AHB-Lite master supporting single and burst transfers (INCR-1,4,8,16,INCR) with automatic HTRANS sequencing and BUSY insertion.
- Designed an AHB-Lite slave with 8-bit × N memory that dynamically collects bursts into byte-wide locations, verifying each beat against HSIZE for correct storage.
- Designed a UVM-based verification environment(Scoreboard Level) with 5 different test sequences.
- Utilized EDA Playground and QuestaSim for simulation and verification.

E2E Scoreboard Design for SPI & APB VIP | *SystemVerilog, UVM, TCL* **GitHub** **March 2025**

- Designed an end-to-end scoreboard for a verification IP comprising BFM, network engine, memory controller, SPI, and APB interfaces.
- Implemented a configurable packet generator class to create address-data patterns across instances and display results in a synchronized 2D memory table for validation.
- Utilized shell scripting to pass multiple parameters and partially automate test execution flow.
- Conducted simulation and verification using EDA Playground, QuestaSim.

64KB Asynchronous RAM Design and Verification | *SystemVerilog, UVM, TCL* **GitHub** **February 2025**

- Designed a 64KB asynchronous RAM supporting parallel read/write and write-after-read operations.
- Developed a UVM testbench up to the scoreboard level to ensure full functional verification.
- Performed simulation and debugging using QuestaSim and EDA Playground environments.

Technical Skills

Languages: Verilog, SystemVerilog, C & C++, Python
Developer Tools: Questasim, Xilinx Vivado, Microwind, EDA Playground, Cygwin, Gvim
Verification Methodologies: SystemVerilog Testbench, UVM Testbench

Certifications

SystemVerilog for Design and Verification - Synopsys
VLSI Digital Design - Chip Design and Verilog programming - Infosys Springboard
RISC-V on FPGA - Cambridge Institute of Technology,BLORE